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Design low-duty-cycle timer circuits

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Designing astable circuits using the industry-standard 555 timer is a straightforward process when duty cycles are 50% or greater. However, you must overcome the many pitfalls of low-duty-cycle circuits to arrive at a desired result. Using only ideal components eases the design, but the components themselves are hard to obtain. Nonideal components get in the way of the easy-to-use standard equations and greatly multiply the tolerances. This Design Idea uses the TLC555 CMOS timer. You can use other versions of the popular 555 timer with appropriate variations in the given parameters. For a standard, greater-than-50%-duty-cycle, low-frequency design (**Figure 1**), you would use the following design equations:

$$t_H = C \cdot (R_A + R_B) \cdot \ln(2);$$

$$t_L = C \cdot R_B \cdot \ln(2);$$

$$\text{DUTY CYCLE} = \frac{(R_A + R_B)}{(R_A + 2R_B)}.$$

Charging current for the timing capacitor flows through R_A and R_B until the capacitor voltage reaches the upper threshold voltage of $0.667V_{CC}$. The capacitor then discharges through R_B and an internal transistor to the lower threshold voltage of $0.333V_{CC}$. Because R_B is present in both the charging and the discharging cycles, you can't implement duty cycles lower than 50% in this configuration. These idealized equations also ignore several factors that slightly degrade the results for the higher range of duty cycles but greatly influence the results of low-duty-cycle designs. These factors include propagation delays and the on-resistance of the internal discharge transistor. All these factors are supply-voltage-dependent. Another factor for low-duty-cycle designs that does not apply to high-duty-cycle designs is the effect of the R_B bypass diode, D_1 (**Figure 2**), required to implement the design.

Adding a bypass diode across R_B allows for designs with duty cycles lower than 50%. During the charging cycle, current flows through R_A and bypasses R_B through the diode. During discharge, current flows through R_B and the internal discharge transistor as usual. Because R_B is now present only in the discharge cycle, you can tailor the duty cycle to any desired point over the full range. Again, using ideal components, the timing equations are simple:

$$t_H = C \cdot R_A \cdot \ln(2);$$

$$t_L = C \cdot R_B \cdot \ln(2);$$

$$\text{DUTY CYCLE} = \frac{(R_A)}{(R_B)}.$$

The factors you must consider in obtaining a design that agrees with calculations include the:

- diode forward voltage,
- propagation delays,

- discharge-transistor on-resistance,
- ratio of R_A to on-resistance, and
- leakage resistance of the control-pin capacitor.

Diode forward voltage depends on the current flowing through the diode. This current can range from a few hundred microamps to tens of milliamps. For a fixed design, you can obtain this voltage from manufacturers' curves or actual measurements you make by applying the desired current through the diode. You can also use the diode equation:

$$I = I_S(e^{qV/kT} - 1).$$

Or, in terms of voltage:

$$V_F = \frac{1}{0.026} \cdot \ln\left(1 + \frac{I}{I_S}\right) =$$

$$38.46 \cdot \ln\left(1 + \frac{I}{I_S}\right).$$

This voltage subtracts from the charging voltage during the charging cycle and affects the charge-ramp time. Propagation-delay times from the THRES (threshold) and TRIG (trigger) inputs to DISCH (discharge) add directly to the period. These delays depend upon supply voltage. The formulas for the propagation delays (in nanoseconds) are:

$$T_{PHL} = -0.0162V_{CC}^5 + 0.8207V_{CC}^4 - 16.205V_{CC}^3 + 155.62V_{CC}^2 - 31.88V_{CC} + 1558; T_{PLH} = -0.0102V_{CC}^5 + 0.5044V_{CC}^4 - 9.6825V_{CC}^3 + 89.622V_{CC}^2 - 401.04V_{CC} + 807.97.$$

Discharge-transistor on-resistance also varies with supply voltage. This resistance affects the discharge current. Also, when you use low-value resistors for R_A (for low-duty-cycle designs), the combination of R_A and the on-resistance yields a voltage divider that affects the discharge voltage. The on-resistance formula for resistance in ohms is:

$$R_{ON} = 59.135V_{CC}^{-0.8101}.$$

Typically, you'd place a small capacitor on the control pin that connects to the upper internal-divider node. This capacitor has only a slight effect on the threshold-trigger voltages. The leakage resistance of the ceramic capacitor is approximately 9 M Ω . This value is high but still accounts for approximately a 1.5% drop in the trigger voltages because of the 80-k Ω divider resistors that the window-comparator circuit uses. When you take all the cited parameters into account, the design equations become considerably more complicated:

$$t_H = C \cdot R_A \cdot$$

$$\ln\left[3 - e^{-t_{PHL}/(R_{ON} \cdot C)}\right] \cdot \left(\frac{2 \cdot V_{CC}}{(2 \cdot V_{CC} - 3 \cdot V_F)}\right) +$$

$$t_{PHL};$$

$$t_L = C \cdot (R_B + R_{ON}) \cdot$$

$$\ln(3 - e^{-t_{PHL}/(C \cdot R_A)}) \cdot 2.38 \cdot$$

$$\left(1 - \frac{1 - \left(\frac{3 \cdot R_{ON}}{(R_A + R_{ON})} \right)}{2 - \left(\frac{3 \cdot R_{ON}}{(R_A + R_{ON})} \right)} \right) + t_{PLH}.$$

These equations include all the known parameters to obtain a nominal design using the TLC555 timer. Tolerances in each of the parameters cause additional variations that you must consider. In addition, you must consider the effects of temperature variations. After you obtain all this knowledge, the simple 555 timer presents a major math problem. However, thanks to modern computers, you can eliminate much of this tedious math using an Excel spreadsheet. It shows the results of calculations both with and without the bypass diode and includes the tolerancing parameters. [Click here](#) to download a zip file that contains the spreadsheet.

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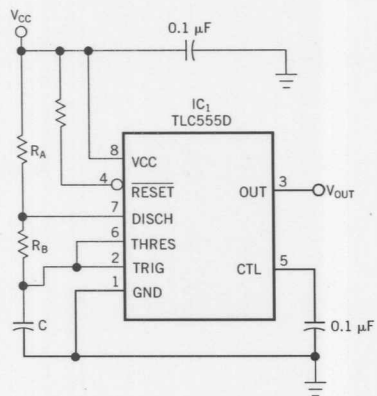


Figure 1

This classic 555-based timer is valid only for duty cycles greater than 50%.

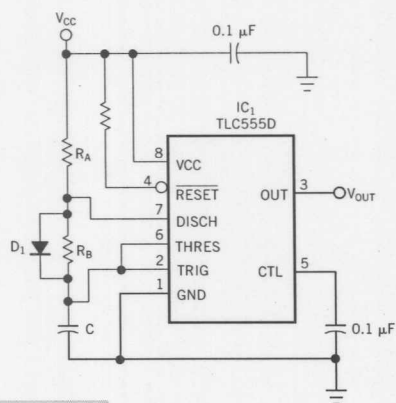


Figure 2

The simple addition of a bypass diode makes this timer circuit valid for low duty cycles.